ABSTRACT OF THE DISCLOSURE

A system and method are disclosed to add logic to the self-refresh control logic presently employed in DRAM devices to ensure that, upon transitions between self-refresh mode and operational mode, at least one row of memory cells due to be refreshed is refreshed during the wait state following issuance of the transition command. Conducting this refresh during this existing wait state eliminates both the concern as to whether rows have been refreshed within the mandated refresh interval and the time required to execute an auto-refresh of at least one row upon completion of the transition.